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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,044	06/24/2003	Takekazu Tanaka	8053-1015	1342

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EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,044	TANAKA, TAKEKAZU	
	Examiner	Art Unit	
	Alonzo Chambliss	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *18-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-17 in the reply filed on 12/29/04 is acknowledged. Claims 18-22 have been cancelled.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 6/24/03 was filed before the mailing date of the non-final rejection on 3/15/05. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

4. The formal drawings filed on 6/24/03 are approved by the examiner.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: " ENCAPSULATED MOSFET CHIP ATTACHED TO A LEAD FRAME ".

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1–17 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Takahashi et al. (JP 2000-049184).

With respect to Claim 1, Takahashi teaches at least one plate-like mount 3 and a semiconductor chip 7 having at least one electrode 11 formed on a top surface thereof. The chip 7 is mounted on the plate like mount 3 such that a bottom surface is in contact with the plate-like mount 3. At least one lead element 5 having an outer portion 6 arranged to be flush with the plate-like mount, and an inner portion 20 deformed and shaped to overhang the semiconductor chip 7 such that an inner end 20 of the lead element 5 is spaced apart from the top surface of the semiconductor chip 7. A bonding-wire element 14 is bonded at ends thereof to the electrode 11 of the semiconductor chip 7 and the inner end 20 of the lead element 5. An enveloper 2 sealing and encapsulating the plate-like mount 3, the semiconductor chip 7, the inner portion 20 of the lead element 5, and the bonding-wire element 14 (see English abstract, paragraphs 54-63, 80-91, and 99-151; Figs. 1-4, 8-13, 17-30).

With respect to Claim 2, Takahashi teaches wherein the electrode is defined as a first electrode and the lead element is defined as a first lead element. The semiconductor chip further having a second electrode 12 formed on the top surface

thereof. The semiconductor package further comprising a second lead element having an outer portion arranged to be flush with the plate-like mount and an inner portion deformed and shaped to overhang the semiconductor chip such that an inner end of the second lead element is directly and electrically connected to the second electrode 12 of the semiconductor chip (see Figs. 1-4, 8-13, 17-30).

With respect to Claims 3, 4, 7, 8, 10-12, 15, and 16, Takahashi teaches wherein the semiconductor chip is constructed as a MOSFET or diode chip having a drain electrode formed on a bottom surface thereof and electrically connected to the plate like mount with the respective first and second electrodes being defined as a source electrode and a gate electrode. The plate-like mount has at least one lead element extending therefrom. The MOSFET chip is formed as a high power type, and the source or anode electrode has a larger area than that of the gate or cathode electrode (see English translation, paragraphs 21, 22, 56-59, and 95; Figs. 1-4, 8-13, 17-30).

With respect to Claims 5, 9, 13, and 17, Takahashi teaches wherein the sealing and encapsulation of the plate like mount in the enveloper is carried out such that a bottom surface of the plate like mount is exposed to outside (see Figs. 1,2, 17, and 21).

With respect to Claims 6 and 14, Takahashi teaches wherein the electrode is defined as and the lead element is defined as a first a first electrode, lead element, the semiconductor chip further having a second electrode formed on the top surface thereof, the semiconductor package further comprising: a second lead element having an outer portion arranged to be flush with the plate-like mount, and an inner portion deformed and shaped to overhang the semiconductor chip such that an inner end

the second lead element spaced apart from the top surface of the semiconductor chip; and at least one bonding-wire element bonded at ends thereof to the electrode of the semiconductor chip and the inner end of the second lead element (see Figs. 1-4, 8-13, 17-30).

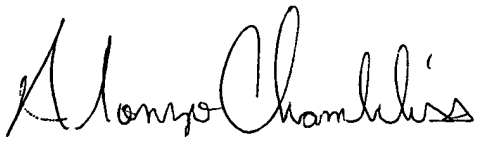
The prior art made of record and not relied upon is cited primarily to show the product of the instant invention.

Conclusion

8. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.



Alonzo Chambliss
Primary Patent Examiner
Art Unit 2814

AC/March 15, 2005